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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,618	INOUE, TOSHIAKI	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-11* is/are rejected.

7)☒ Claim(s) *5-7 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1-5 and 8-12 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see pages 9-13, filed October 12, 2005, with respect to the rejection(s) of claim(s) 1 under 35 U.S.C. 102(e) and claims 2-4 and 8-11 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Applicant's Admitted Prior Art in view of Toksvig (US006870542B2).

3. Applicant's arguments, see page 11, filed October 12, 2005, with respect to Claims 5-7 and 12-14 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejections of Claims 5-7 and 12-14 has been withdrawn.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) (Figures 5A, 5B, 5C, and 6 and respective areas of the specification) in view of Toksvig (US006870542B2).

7. With regard to Claim 1, APA describes a digital image processing device for signal-processing a video input signal and supplying a video input signal and supplying a video output signal to a display panel, comprising a signal processing unit (602, Figure 6) to process this video input signal; a redundant pixel embedding circuit (603) to embed data as redundant pixels into an image line read from the signal processing section. The image line in which dummy data is embedded, after having been stored in a frame memory (604), is transferred to the driver (605) and the driver outputs a video signal (page 3, lines 3-12).

However, APA does not teach that the processed video input signal from the signal processing unit is first stored in the frame memory, and a driver including a redundant pixel embedding circuit embeds data as redundant pixels into an image line read from the frame memory. However, Toksvig describes that the processed video input signal from the signal

processing unit (410, Figure 4) is first stored in the frame memory (415; Col. 5, lines 59-58), and the driver (420) including a filter (430) filters the graphics data read from the frame memory (Col. 6, lines 3-14).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of APA so that the processed video input signal from the signal processing unit is first stored in the frame memory, and a driver including a redundant pixel embedding circuit embeds data as redundant pixels into an image line read from the frame memory as suggested by Toksvig. Toksvig suggests that having a driver including a filter to filter the graphics data read from the frame memory allows for filtering of oversampled data during scanout operation, which has the advantage of filtering oversampled data without requiring additional memory or memory access operation (Col. 2, lines 44-57). Since Toksvig suggests this advantage, it would be obvious to modify the device of APA so that the driver includes the redundant pixel embedding circuit to embed data as redundant pixels into an image line read from the frame memory in order to have the advantage of embedding redundant pixels without require additional memory or memory access operations.

8. With regard to Claim 8, Claim 8 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

9. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figures 5A, 5B, 5C, and 6 and respective areas of the specification) and Toksvig (US006870542B2) in view of O'Sullivan (US005896140A).

10. With regard to Claim 2, APA and Toksvig are relied upon for the teachings as discussed above relative to Claim 1. APA describes a redundant pixel embedding circuit (603, Figure 6; page 3, lines 5-8).

However, APA does not teach that the redundant pixel embedded circuit receives, as an input, an image line read from the frame memory. However, Toksvig describes that the filter (430, Figure 4) has a function of receiving, as an input, an image line read from the frame memory (415; Col. 6, lines 3-12). Therefore, it would be obvious to modify the device of APA so that the redundant pixel embedded circuit receives, as an input, an image line read from the frame memory, as discussed in the rejection for Claim 1.

However, APA and Toksvig do not specifically teach that the redundant pixel embedding circuit has a function of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in the image line. However, O'Sullivan describes that the redundant pixel embedding circuit (44, Figure 2) has a function of receiving, as an input, an image line (Col. 12, line 65-Col. 13, line 1) read from the signal processing unit (42; Col. 7, lines 17-24) and of embedding, according to an embedding control signal fed from outside (*frame grabber controller 52 provides the dummy pixel value to the dummy pixel logic 53, which controls the clocking in of data from the decoder/scaler 44 to provide the proper number of dummy video pixels before each horizontal scan line of video pixels*, Col. 15, lines 20-26), a redundant pixel in a specified position in the image data (Col. 14, line 56-Col. 15, line 6).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of APA and Toksvig so that the redundant pixel embedding

circuit has a function of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in the image line as suggested by O'Sullivan because O'Sullivan suggests that this is needed in order to prevent losing video pixels and/or restrict the placement of a video window on the computer screen (Col. 2, lines 62-65; Col. 14, line 33-67).

11. With regard to Claim 9, Claim 9 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

12. Claims 3, 4, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figures 5A, 5B, 5C, and 6 and respective areas of the specification) in view of Toksvig (US006870542B2), further in view of Mori (US005060059A).

13. With regard to Claim 3, Claim 3 is similar in scope to Claim 1, with the addition of a serial-parallel converting circuit and a parallel-serial converting circuit. Therefore, Claim 3 is rejected under the same rationale as Claim 1.

However, APA and Toksvig do not teach that the device includes a serial-parallel converting circuit and a parallel-serial converting circuit. However, Mori describes a digital image processing device comprising a signal processing unit (110, Figure 6) to process a video input signal (100; Col. 5, lines 19-25); a serial-parallel converting circuit (201) to receive image data read from signal processing unit (Col. 5, lines 24-39). Mori describes that the image data from the signal processing unit is color-sequential color image data, and it is supplied to a time base conversion unit 200a which converts the frequency of the image data (Col. 5, lines 24-34). Since the data is sequential and has a frequency, the serial-parallel converting circuit receives the

data in a time-series manner (Col. 5, lines 30-39) and produces an output (Col. 5, lines 36-39). The output from the serial-parallel converting circuit is input into a line buffer (207), as can be seen in Figure 6, and therefore the serial-parallel converting circuit produces an output making up an image line. Mori describes that the output from the serial-parallel converting circuit (201, Figure 6; 10, Figure 1) is input into the adder (17; Col. 4, lines 9-42), and the adder receives dummy data (Col. 4, lines 49-52). The output of the adder is input into a parallel-serial converting circuit (241, Figure 14; 211, Figure 6; 5, Figure 1; Col. 4, lines 49-56; Col. 9, lines 49-55), which outputs the image line in which the dummy data is embedded as color-sequential image data or time-series image data (Col. 9, lines 50-65).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of APA and Toksvig so that the device includes a serial-parallel converting circuit and a parallel-serial converting circuit as suggested by Mori because Mori suggests that data converters for conversion of color-sequential image data into parallel data in the masking circuit and in the black extraction circuit where parallel image data are needed, and effects image processing on color-sequential image data in other sections have the advantages of reducing the number of circuit components and compactizing the apparatus; and reducing the cost of the color image processing apparatus (Col. 5, lines 4-15).

14. With regard to Claim 4, APA and Toksvig do not teach a serial-parallel converting circuit which is made up of a register file being able to store an image line and which has a function of sequentially storing image data fed from the frame memory in a time-series manner according to a writing control signal fed from outside and of reading, simultaneously and in parallel, contents

of all registers in the register file. However, Mori describes that the serial-parallel converting circuit (201, Figure 6; 10, Figure 1) which is made up of a register file (40-44, Figure 5) being able to store an image line and which has a function of sequentially storing image data (7) fed from the signal processing unit (110, Figure 6; 1, Figure 1; Col. 3, lines 38-45) according to a writing control signal (46, Figure 5) fed from outside (45; *latch controller 45 for releasing latch signals 46 for the registers in response to the mode signal 6 and the clock signal 8*, Col. 4, line 58-Col. 5, line 3). Since the latch signal is controlled by the clock signal, the image data is fed in a time-series manner. Mori describes that the serial-parallel converting circuit reads, simultaneously and in parallel, contents of all registers in the register file (*data converter releases 8-bit color image data in parallel manner*, Col. 5, lines 2-3). This would be obvious for the same reasons given in the rejection for Claim 3.

15. With regard to Claim 10, Claim 10 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

16. With regard to Claim 11, Claim 11 is similar in scope to Claim 4, and therefore is rejected under the same rationale.

Allowable Subject Matter

17. Claims 5-7 and 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

18. The prior art taken singly or in combination do no teach or suggest a digital image processing device according to Claim 3, wherein the redundant pixel embedding circuit has a function of receiving, as an input the image line read from the serial-parallel converting circuit and of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in the image line, as suggested by Claims 5 and 12. The prior art also does not teach that the digital image processing device according to Claim 3, wherein the parallel-serial converting circuit has a register file made up of two or more shift registers, as recited in Claims 6 and 13. Claims 7 and 14 depend from these claims, and therefore also contain allowable subject matter.

19. The closest prior art (Hayashi US005305122A) teaches that the parallel-serial converting circuit (7, Figure 3) has a register file made up a shift register (*shift register 7 is a 16-bit parallel-serial converte*r, Col. 9, lines 25-29) and a selector (9) to select an output from the shift register and to output the selected output (*selector 9 selects either the output from the shift register 7 or a signal at ground voltage "0" as an output VD*, Col. 7, lines 1-3) and wherein the register file is able to store an image line in one clock cycle (Col. 13, lines 45-47) and wherein the shift register is able to perform a shifting operation, according to a reading control signal fed from outside, in synchronization with a clock signal (20; Col. 7, lines 4-10) and wherein the selector (31, Figure 9) has a function of selecting a specified shift output from the shift register and of outputting the selected output according to an embedding control signal fed from outside

(32; Col. 8, lines 31-35). However, Hayashi does not teach that the register is file is made up of two or more shift registers.

20. Another prior art (Heilveil US004639890A) teaches that the parallel-serial converting circuit (a serial shift register for interconnection in parallel with the columns of cells, Col. 2, lines 46-48) has a register file (20, Figure 3) made up of two or more shift registers (*shift register 20 split into two identical halves*, Col. 6, lines 18-22) and a selector (26, Figure 2) to select an output from each of the shift registers and to output the selected output (Col. 6, lines 34-37) and wherein each of the shift registers is able to perform a shifting operation, according to a reading control signal fed from outside, in synchronization with a clock signal (*shift register 20 is operated by a clock which is used to shift the bits through the stages of the register*, Col. 6, lines 38-46). However, Heilveil does not teach a redundant pixel embedding circuit.

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Hayashi (US005305122A) teaches an image processing apparatus which can perform transmission in a simple transmission form with transmitting a color image (Col. 5, lines 7-10).

2. Heilveil (US004639890A) teaches a serial shift register for interconnection in parallel with the columns of cells (Col. 2, lines 41-53).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner